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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,398	12/05/2003	William C. Moyer	SC13064TH	9268

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EXAMINER	
MEHRMANESH, ELMIRA	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 12/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/728,398	MOYER ET AL.	
	Examiner	Art Unit	
	Elmira Mehrmanesh	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to an amendment filed on September 26, 2006 for the application of Moyer et al., for "Apparatus and method for time ordering events in a system having multiple time domains" filed December 5, 2003.

Claims 11-45 are pending in the application.

Claim 45 is rejected under 35 USC § 102.

Claims 11-44 are rejected under 35 USC § 103.

Claims 1-10 have been cancelled.

Claims 35-45 have been added.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 11-24, 26-34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Edwards (U.S. Patent No. 6,487,683) in view of Steinberg et al. (U.S. Patent No. 6,966,015).

As per claim 11, Edwards discloses a system for time ordering events comprising: a plurality of functional circuit modules (Fig. 8) each functional circuit module (Fig. 10A, elements 200A-F) the timestamping circuitry providing a message that indicates a point in time when a predetermined event occurs (Fig. 6D, element 148)

an interface module coupled to each of the plurality of functional circuit modules, the interface module providing control information to the plurality of functional circuit modules to indicate at least one operating condition that triggers (Fig. 10B, elements 180A-F) the predetermined event, the interface module receiving at least one timestamping message from a first time domain when the predetermined event occurs (Fig. 10B, elements 112A-F) in one of a plurality of time domains including the first time domain (Fig. 6D, element 148).

Edwards fails to explicitly disclose different time domains.

Steinberg teaches:

being clocked by a clock that represents a different time domain and having timestamping circuitry (Fig. 2 and Fig. 3, element 44).

It would have been obvious to one of ordinary skill in the art at the time the invention to use the method of System-on-chip debugging of Edward's in

combination with the method of reducing false alarms in network fault management systems of Steinberg et al's to provide debugging information.

One of ordinary skill in the art at the time the invention would have been motivated to make the combination because Edwards discloses a debugging system for System-on-chip devices (Fig. 1). Steinberg et al. discloses a method of correlating event data in different time slices (Fig. 1).

As per claim 12, Edwards discloses the interface module further comprises: storage circuitry for storing the control information (Fig. 10B, elements 112A-F) as programmable control information that determines (col. 19, lines 22-24) the at least one operating condition that triggers the predetermined event (col. 13, lines 57-65).

As per claim 13, Edwards discloses the at least one operating condition that triggers the predetermined event further comprises at least one of: entrance into or exit from a power mode of operation, a change in source of a clock, a change in clock periodicity, a predetermined change in a hardware counter value, entry into and exit from a debug mode of operation, and occurrence of at least one user programmable event (col. 7, lines 61-67 through col. 8, lines 1-9).

As per claim 14, Edwards discloses the timestamping circuitry further comprises: a counter for determining either absolute or relative time in a corresponding functional circuit module (Fig. 6E, element 154)

time domain identification circuitry for providing a time domain identifier (Fig. 5A, elements 122, 126)

clock status circuitry for providing one or more operating characteristics of a clock in the corresponding functional circuit module (Fig. 9).

As per claim 15, Edwards discloses the timestamping circuitry further comprises circuitry for generating a code to be included in each message to identify a format of information included in a corresponding message (Fig. 6D, element 146).

As per claim 16, Edwards discloses the interface module further comprises an arbiter having circuitry for generating a code to be included in each timestamping message to identify a format of information (Fig. 6D, element 146) included in a corresponding timestamping message (Fig. 6D, element 148).

As per claim 17, Edwards discloses the message provided by at least one of the plurality of functional circuit modules (Fig. 10A) has a format that comprises at least a time count value (Fig. 6E, element 154) that is an absolute value referenced to a known starting value, status information of a clock signal associated with one of the functional circuit modules (col. 19, lines 38-46) and an identifier that indicates a corresponding time domain associated with the timestamping message (Fig. 6D, element 148).

As per claim 18, Edwards discloses the message has a format that further comprises a field that identifies that the format of the timestamping message has an absolute value time count value (Fig. 6D, element 146, 148) and (Fig. 6E, element 154).

As per claim 19, Edwards discloses the message provided by at least one of the plurality of functional circuit modules (Fig. 10A) has a format that comprises at least a time count value (Fig. 6E, element 154) that is a relative value referenced to a last occurring predetermined event, status information of a clock signal associated with one of the functional circuit modules (col. 19, lines 38-46) and an identifier that indicates a corresponding time domain associated with the timestamping message (Fig. 6D, element 148).

As per claim 20, Edwards discloses the message has a format that further comprises a field that identifies that the format of the timestamping message having a relative value time count value (Fig. 6D, element 146, 148) and (Fig. 6E, element 154).

As per claim 21, Edwards discloses the timestamping message has a format that comprises a time count value corresponding to each of the functional circuit modules and predetermined status information associated with each of the functional circuit modules when the predetermined event occurs (Fig. 6D,

element 146, 148) and (Fig. 6E, element 154).

As per claim 22, Edwards discloses the control information is programmable (col. 19, lines 22-24).

As per claim 23, Edwards discloses the interface module further comprises: at least one register for storing the control information (Fig. 10B, elements 112A-F).

As per claim 24, Edwards discloses the interface module provides timestamping messages from all time domains at a common interface port (Fig. 10A).

As per claim 26, Edwards discloses a system for time ordering events comprising: a plurality of functional circuit module (Fig. 8) means, the timestamping circuit means providing a message that indicates a point in time when a predetermined event occurs (Fig. 6D, element 148)

interface module means coupled to each of the plurality of functional circuit module means (Fig. 10B, elements 180A-F) the interface module means providing control information to the plurality of functional circuit module means to indicate at least one operating condition that triggers the predetermined event (Fig. 10B, elements 180A-F) the interface module means receiving at least one timestamping message from a first time domain when the predetermined event

occurs (Fig. 10B, elements 112A-F) in one of a plurality of time domains including the first time domain (Fig. 6D, element 148).

Edwards fails to explicitly disclose different time domains.

Steinberg teaches:

being clocked by a clock that represents a different time domain and having timestamping circuitry (Fig. 2 and Fig. 3, element 44).

As per claim 27, Edwards discloses the timestamping messages from all time domains are provided by interface module means at a common interface port means (Fig. 10A).

As per claim 28, Edwards discloses a system comprising: a plurality of functional circuit modules (Fig. 8 and 10A-B) on a same integrated circuit (col. 4, lines 16-18), each functional circuit module being clocked by a clock (Fig. 9, element 205) and each functional module having timestamping circuitry operating at independent clock rates for providing timestamp messages (Fig. 6D, element 148).

Edwards fails to explicitly disclose different time domains.

Steinberg teaches:

being clocked by a clock that represents a different time domain and having timestamping circuitry (Fig. 2 and Fig. 3, element 44).

As per claim 29, Edwards discloses the timestamp messages each indicate a point in time when a predetermined event occurs (Fig. 6D, element 148).

As per claim 30, Edwards discloses an interface module coupled to each of the plurality of functional circuit modules (Fig. 10B, elements 180A-F) the interface module providing control information to the plurality of functional circuit modules to indicate at least one operating condition that triggers the predetermined event (Fig. 10B, elements 180A-F) the interface module receiving at least one timestamping message (Fig. 6D, element 148) from a first time domain when the predetermined event occurs in one of a plurality of time domains including the first time domain (Fig. 6E, element 156).

As per claim 31, Edwards discloses a method of reconstructing time ordering of events that occur in multiple time domains in a system, the method comprising: receiving multiple timestamping messages (Fig. 6D, element 148) in one of an ordered time sequence and an unordered time sequence; tracking relative count values of multiple time domain counters (Fig. 5B, element 126) and (Fig. 6E, element 156) and (Fig. 6F, element 158) associated with the multiple time domains and operating at independent clock rates; and sorting debug information in time ordered sequence, the debug information being associated with a timestamp (Fig. 6D, element 148).

Edwards fails to explicitly disclose different time domains.

Steinberg teaches:

A timestamp provided from one of the multiple time domains (Fig. 2 and Fig. 3, element 44).

As per claim 32, Edwards discloses providing the debug information via a debug message (Fig. 3, elements 72, 32).

As per claim 33, Edwards discloses implementing the debug messages as at least one of a program trace message, a data trace message and a watchpoint message (Fig. 3) and (col. 14, lines 34-52).

As per claim 34, Edwards discloses generating the multiple timestamp messages (Fig. 6D, element 148) by: providing control information corresponding to each of multiple time domains (Fig. 6C, 6D), the control information indicating when a timestamp message for each of the multiple time domains is to be generated (Fig. 6D, element 148) determining when a time domain event that requires generation of a timestamp message occurs in any one of the multiple time domains (Fig. 6E, element 154) and generating a timestamp message corresponding to a predetermined one of the multiple time domains in response to determining that the time domain event occurred (Fig. 6D, element 148).

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Edwards (U.S. Patent No. 6,487,683) in view of Steinberg et al. (U.S. Patent No. 6,966,015) and in further view of Rohfleisch et al. (U.S. Patent No. 7,058,855).

As per claim 25, Edwards in view of Steinberg fails to explicitly disclose IEEE ISTO 5001 (NEXUS).

Rohfleisch teaches:

the common interface port of the interface module meets IEEE ISTO 5001 (NEXUS) compliance (col. 7, lines 65-67 through col. 8, lines 1-8).

It would have been obvious to one of ordinary skill in the art at the time the invention to use the method of System-on-chip debugging of Edward's in combination with the on-chip debugging system of Rohfleisch et al. to provide debugging information.

One of ordinary skill in the art at the time the invention would have been motivated to make the combination because Edwards discloses a debugging system for System-on-chip devices (Fig. 1). Rohfleisch et al. teaches of the on-chip debugging system of integrated circuit (Fig. 1) and (col. 7, lines 60-65). Edwards uses the method of generating timestamp messages to identify events (Fig. 6D, element 148). Rohfleisch et al. also discloses a method of using timestamps (col. 8, lines 9-22).

Claims 35-41, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steinberg et al. (U.S. Patent No. 6,966,015) and in view of Chen et al. (U.S. Patent No. 5,642,478).

As per claim 35, Steinberg discloses a method for providing debug information to debug an integrated circuit, the method comprising:

a first clock that represents a first time domain, the first functional circuit module providing a first timestamp which indicates a point in time when a first predetermined event occurs (Fig. 3)

a second clock that represents a second time domain, the second functional circuit module providing a second timestamp which indicates a point in time when a second predetermined event occurs (col. 8, lines 1-55)

providing a first debug message, the first debug message comprising the first timestamp which indicates the point in time when the first predetermined event occurred (col. 8, lines 1-55)

providing a second debug message, the second debug message comprising the second timestamp which indicates the point in time when the second predetermined event occurred (col. 8, lines 1-55)

providing a third debug message, the third debug message comprising timestamp information from the first functional circuit module and timestamp information from the second functional circuit module (col. 8, lines 1-55)

wherein the timestamp information from the first functional circuit module and the timestamp information from the second functional circuit module were collected at approximately a same point in time (Fig. 1, element 22)

and wherein a difference between the timestamp information from the first functional circuit module and the timestamp information from the second functional circuit module can be used in conjunction with the first timestamp and the second timestamp to determine whether the first predetermined event or the second predetermined event occurred first (Fig. 3, element 44) and (col. 8, lines 1-55).

Steinberg fails to teach multiple integrated circuits.

Chen et al. teaches:

first functional circuit module on the integrated circuit, providing a second functional circuit module on the integrated circuit (Fig. 1, element 54).

It would have been obvious to one of ordinary skill in the art at the time the invention to use the method of reducing false alarms in network fault management systems of Steinberg et al's in combination with the distributed trace data acquisition system of Chen et al.

One of ordinary skill in the art at the time the invention would have been motivated to make the combination because Steinberg et al. discloses a method of correlating event data in different time slices (Fig. 1). Chen et al. discloses capturing event data for software and hardware debugging (Fig. 1).

As per claim 36, Steinberg discloses wherein the first timestamp comprises a value from a counter in the first functional circuit module, wherein the counter is clocked by the first clock (col. 9, lines 7-19).

As per claim 37, Steinberg discloses wherein the first timestamp comprises a value representing a difference between a first value and a second value from a counter in the first functional circuit module, wherein the second value was captured when the first predetermined event occurred, and the first value was captured before the first predetermined event occurred (col. 9, lines 7-19).

As per claim 38, Steinberg discloses wherein the first debug message further comprises information regarding status of the first clock (Fig. 3, element 44) and (col. 6, lines 49-65).

As per claim 39, Steinberg discloses including within the first debug message a format identifier field that identifies one of a plurality of predetermined formats that the timestamp message has (Fig. 3).

As per claim 40, Steinberg discloses wherein the first debug message further comprises information regarding which time domain is providing the first timestamp (Fig. 3).

As per claim 41, Steinberg discloses wherein the first functional circuit module provides the first timestamp to indicate the point in time when the first predetermined event occurred, and wherein the first predetermined event actually occurred in the second functional circuit module (col. 8, lines 1-55).

As per claim 44, Steinberg discloses a method as in claim 35, wherein the first predetermined event comprises at least one of entrance into or exit from a power mode of operation, a change in source of a clock, a change in clock periodicity, a predetermined change in a hardware counter value or entry into and exit from a debug mode of operation (col. 9, lines 7-19).

Claims 42-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steinberg et al. (U.S. Patent No. 6,966,015) and in view of Chen et al. (U.S. Patent No. 5,642,478) and further view of Rohfleisch et al. (U.S. Patent No. 7,058,855).

As per claim 42, Steinberg view of Chen fails to explicitly disclose an IEEE ISTO 5001 (NEXUS).

Rohfleisch teaches:

wherein a format of the third debug message meets IEEE ISTO 5001 (NEXUS) compliance (col. 7, lines 65-67 through col. 8, lines 1-8).

It would have been obvious to one of ordinary skill in the art at the time the invention to use the method of reducing false alarms in network fault

management systems of Steinberg et al's in combination with the on-chip debugging system of Rohfleisch et al. to provide debugging information.

One of ordinary skill in the art at the time the invention would have been motivated to make the combination because Steinberg et al. discloses a method of correlating event data in different time slices (Fig. 1). Rohfleisch et al. teaches of the on-chip debugging system of integrated circuit (Fig. 1) and (col. 7, lines 60-65). Edwards uses the method of generating timestamp messages to identify events (Fig. 6D, element 148). Rohfleisch et al. also discloses a method of using timestamps (col. 8, lines 9-22).

As per claim 43, Steinberg view of Chen fails to explicitly disclose an IEEE ISTO 5001 (NEXUS).

Rohfleisch teaches:

wherein the first debug message and the second debug message have a format, which meets IEEE ISTO 5001 (NEXUS) compliance (col. 7, lines 65-67 through col. 8, lines 1-8).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for

> patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 45 is rejected under 35 U.S.C. 102(e) as being anticipated by Steinberg et al. (U.S. Patent No. 6,966,015).

As per claim 45, Steinberg discloses a method for operating an integrated circuit, comprising:

providing a plurality of time domains in the integrated circuit (Fig. 2 and Fig. 3, element 44)

timestamping events happening in the plurality of time domains (Fig. 3)

correlating the events happening in the plurality of time domains using the timestamping (Fig. 1, element 22) and using the correlating of the events happening in the plurality of time domains to perform debugging of the integrated circuit (Fig. 3).

Response to Arguments

Applicant's arguments have been fully considered with the examiner's response detailed below.

Applicant's arguments see pages 10-12, filed September 26, 2006 with respect to the rejection(s) of claim(s) 1-34 under 35 USC § 102 and 35 USC § 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made over Edwards (U.S. Patent No. 6,487,683) in view of Steinberg

et al. (U.S. Patent No. 6,966,015) and in further view of Chen et al. (U.S. Patent No. 5,642,478) and Rohfleisch et al. (U.S. Patent No. 7,058,855). Refer to the corresponding section of the claim analysis for details.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elmira Mehrmanesh whose telephone number is (571) 272-5531. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).